Abstract

An analog-to-digital converter in which each of a plurality of comparators is, in a successive approximation manner, selectively enabled or disabled and the outputs from those comparators summed together to produce a digital signal therefrom. By weighting and mixing outputs of adjacent comparators in proportions calculated to provide an interpolated output of a virtual comparator between the actual comparators, many such virtual comparators can be created without the need for additional fixed hardware elements in the converter. By doing so, the converter is able to produce a digital output having n bits using only N actual hardware elements for comparing signals, where $N < 2^n - 1$. Each of the plurality of comparators in the converter has an input for an enabling signal, which enabling signal can be manipulated to enable or disable individual comparators and to modify their outputs. A method for converting an analog input signal into a digital signal using such a converter.